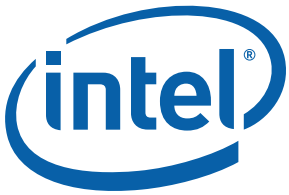


Intel® I/O Controller Hub 9 (ICH9) Family

Specification Update

— For the Intel® 82801IB ICH9, 82801IR ICH9R, and 82801IH ICH9DH, 82801IO ICH9DO I/O Controller Hubs

June 2008

Notice: The Intel® I/O Controller Hub 9 (ICH9) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Order Number: 316973-009

Contents

Revision History

Revision	Description	Date
-001	• Initial Release	June 2007
-002	• Added 82801IO ICH9DO specifications • Added following Errata - Errata 4, Intel ICH9 THRM Polarity on SMBus - Errata 5, Intel ICH9 SPI_CS1# State	August 2007
-003	• Added: • - Errata: 6-ICH9 Level-Triggered Legacy IRQ, 7-ICH9 High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level • - Specification Clarifications: 1-GLANCLK High Time/Low Time Clarification	September 2007
-004	• Added: • - Errata: 8-PET Alerts on SMBus • - Specification Changes: 1-t212 Change, 2-LANRST# Timing, 3-Removing Support for USB Wake from S5 • - Specification Clarifications: 2-DC Characteristics Clarifications, 3-USB UHCI Run/Stop Bit Clarification • - Document Changes: 1-PWROK Description Correction, 2-SMBus/SMLink Connectivity Clarification, 3-External RTC Circuit Correction, 4-D31:F6:52h Register Default Value Correction, 5-SPI_CS0# Description Correction, 6-Miscellaneous Register Default Value Corrections	November 2007
-005	• Added: • - Specification Changes: 4-Addition of EHCI Parity Error Response • - Specification Clarifications: 4-BIOS VSCC and Management Engine VSCC Clarifications • - Document Changes:7-Miscellaneous Electrical Correction	February 2008
-006	• Added: • - Errata: 9-SMBus Host Controller May Hang • - Specification Clarifications: 5-Causes of SMI# /SCI Clarifications, 6-SATA Clock Gating Control Register Clarification • - Document Changes: 8-HPET Address Range Correction	March 2008
-007	• Not released, to synchronize with the specification update posting schedule	
-008	• Added: • - Errata: 10-SATA Gen1 Initialization / LPM Erratum • - Specification Changes:5-SATA Port Multipliers Removal, 6-CF9 Lock Bit Addition • - Document Changes: 9-GNT[3:0]# Pull up Enable Correction	May 2008
-009	• Added: • - Specification Clarifications: 7-CLIST1 (D25:F0:Offset C8h-C9h) Register Corrections, 8-EHCI Initialization Register 1 Clarification, 9-PCI Express* Root Port Configuration Register Clarification • - Document Changes: 10-Device 31 Interrupt Pin Register Corrections,11-D31:F0 Capability List Pointer Addition	June 2008

§ §

Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Number
Intel® I/O Controller Hub 9 (ICH9) Family Datasheet	316972-002

Nomenclature

Errata are design defects or errors. These may cause the Product Name's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings	Status	ERRATA
	A2		
1	X	No Fix	Intel® ICH9 UHCI Hang with USB Reset
2	X	No Fix	Intel ICH9 1.5 Gb/s SATA Signal Voltage Level
3	X	No Fix	Intel ICH9 High-speed USB 2.0 V_{HSOH}
4	X	No Fix	Intel ICH9 THRM Polarity on SMBus
5	X	No Fix	Intel ICH9 SPI_CS1# State
6	X	No Fix	Intel ICH9 Level-Triggered Legacy IRQ
7	X	No Fix	Intel ICH9 High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level
8	X	No Fix	PET Alerts on SMBus
9	X	No Fix	SMBus Host Controller May Hang
10	X	No Fix	SATA Gen1 Initialization / LPM Erratum

Specification Changes

No.	Steppings	SPECIFICATION CHANGES
	A2	
1	X	t212 Change
2	X	LANRST# Timing
3	X	Removing Support for USB Wake from S5
4	X	Addition of EHCI Parity Error Response
5	X	SATA Port Multipliers Removal
6	X	CF9 Lock Bit Addition

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	GLANCLK High Time/Low Time Clarification.
2	DC Characteristics Clarifications
3	USB UHCI Run/Stop Bit Clarification
4	BIOS VSCC and Management Engine VSCC Clarifications
5	Causes of SMI# /SCI Clarifications
6	SATA Clock Gating Control Register Clarification
7	CLIST1 (D25:F0:Offset C8h-C9h) Register Corrections
8	EHCI Initialization Register 1 Clarification
9	PCI Express* Root Port Configuration Register Clarification

Documentation Changes

No.	DOCUMENTATION CHANGES
1	PWROK Description Correction
2	SMBus/SMLink Connectivity Clarification
3	External RTC Circuit Correction
4	D31:F6:52h Register Default Value Correction
5	SPI_CS0# Description Correction
6	Miscellaneous Register Default Value Corrections
7	Miscellaneous Electrical Correction
8	HPET Address Range Correction
9	GNT[3:0]# Pull up Enable Correction
10	Device 31 Interrupt Pin Register Corrections
11	D31:F0 Capability List Pointer Addition

§ §

Identification Information

Markings

Stepping	S-Spec	Top Marking	Notes
A2	SLA9M	NH82801IB	Intel® 82801IB ICH9
A2	SLA9N	NH82801IR	Intel® 82801IR ICH9R
A2	SLA9P	NH82801IH	Intel® 82801IH ICH9DH
A2	SLAFD	NH82801IO	Intel® 82801IO ICH9DO

§ §

Intel® ICH9 Device and Revision Identification

ICH9 Device and Revision ID Table

Device Function	Description	Intel® ICH9 Dev ID[1]	ICH9 A2 Rev ID	Comments
	LPC	2912h	02h	ICH9DH
		2914h	02h	ICH9DO
		2916h	02h	ICH9R
		2918h	02h	ICH9
D31:F2	SATA	2920h	02h	Desktop Non-AHCI and Non-RAID Mode (Ports 0,1, 2 and 3)
		2921h	02h	Desktop Non-AHCI and Non-RAID Mode (Ports 0 and 1)
		2922h	02h	Desktop AHCI Mode (Ports 0-5)
		2923h	02h	Desktop AHCI Mode (Ports 0,1,4 and 5)
		2822h[3]	02h	Desktop RAID 0/1/5/10 Mode
D31:F5	SATA	2926h	02h	Desktop Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	2930h	02h	
D31:F6	Thermal	2932h	02h	
D30:F0	DMI to PCI Bridge	244Eh	92h	
D29:F0	USB UHCI #1	2934h	02h	
D29:F1	USB UHCI #2	2935h	02h	
D29:F2	USB UHCI #3	2936h	02h	
D29:F3	USB UHCI #6	2939h	02h	Note: Device and Revision ID is always the same as D26:F2.

ICH9 Device and Revision ID Table

Device Function	Description	Intel® ICH9 Dev ID[1]	ICH9 A2 Rev ID	Comments
D29:F7	USB EHCI #1	293Ah	02h	
D26:F0	USB UHCI #4	2937h	02h	
D26:F1	USB UHCI #5	2938h	02h	
D26:F2	USB UHCI #6	2939h	02h	
D26:F7	USB EHCI #2	293Ch	02h	
D27:F0	Intel® High Definition Audio	293Eh	02h	
D28:F0	PCI Express* Port 1	2940h	02h	
D28:F1	PCI Express Port 2	2942h	02h	
D28:F2	PCI Express Port 3	2944h	02h	
D28:F3	PCI Express Port 4	2946h	02h	
D28:F4	PCI Express Port 5	2948h	02h	
D28:F5	PCI Express Port 6	294Ah	02h	
D25:F0	LAN	29C4h[2]	02h	

NOTES:

1. ICH9 contains two SATA controllers. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the component.
2. Loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 294Ch is used. Refer to the ICH9 NVM Map and Programming Guide for LAN Device IDs.
3. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch.

Errata

1. Intel® ICH9 UHCI Hang with USB Reset

Problem: When SW initiates a Host Controller Reset or a USB Global Reset while concurrent traffic occurs on at least three UHCI controllers, the UHCI controller(s) may hang.

Note: The issue has only been replicated in a synthetic reset test environment.

Implication: System may hang.

Workaround: BIOS workaround available. See latest BIOS Spec Update for details.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

2. Intel® ICH9 1.5 Gb/s SATA Signal Voltage Level

Problem: The ICH9 1.5Gb/s SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the ICH9 SATA 1.5 Gb/s (Gen1i and Gen1m) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specification (section 7.2.1 of Serial ATA Specification, rev 2.5).

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

3. Intel® ICH9 High-speed USB 2.0 V_{HSOH}

Problem: ICH9 High-speed USB 2.0 V_{HSOH} may not meet the USB 2.0 specification.

— The maximum expected V_{HSOH} is 460mV.

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

4. Intel ICH9 THRM Polarity on SMBus

Problem: When THRM#_POL (PMBASE+42h:bit0) is set to high, the THRM# pin state as reported to the SMBus TCO unit is logically inverted.

Implication: If the THRM#_POL bit is set to high, an external SMBus master reading the BTI Temperature Event status will not receive the correct state of the THRM# pin. The value will be logically inverted. If THRM#_POL is set to low, value is correct.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

5. Intel ICH9 SPI_CS1# State

Problem: After resuming from S3-S5, the ICH9 SPI_CS1# signal may initially drive a low voltage on the pin.

Implication: If only one SPI device is populated on the system, there is no impact.
If two SPI devices are populated, system may hang when resuming from S3-S5.

- When the ICH9 performs its initial read to the SPI device on SPI_CS0#, SPI_CS1# could also be asserted. BIOS may not receive correct boot data.

Workaround: Available.

1) For ME-enabled systems:
- Desktop: use ME firmware version 3.0.2.xxxx or later, or populate one SPI device.

2) For non-ME systems: populate one SPI device.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

6. ICH9 Level-Triggered Legacy IRQs

Problem: When the ICH9 legacy interrupts [15:0] are configured as level triggered interrupts, the ICH9 may invert the default interrupt level from high-active to low-active.

Implication: Devices or Virtualization SW stacks which use legacy interrupts [15:0] as low-active level-triggered on the system may see performance degradation due to excessive IRQ requests.

Note: Intel has not identified any impacted devices or production virtualization system software stacks (VMMs/OS).

Workaround: Available.

- For impacted devices: BIOS or Device Driver ensures the ICH9 legacy interrupts [15:0] are configured as edge triggered.
- For impacted Virtualization SW stacks:
  - Option 1: Virtualization SW to configure ICH9 legacy interrupt [15:0] as edge triggered
  - Option 2: Virtualization SW should mask the low active level triggered interrupt allocated to the virtual interrupt by executing the following steps:
    . Check if platform is ICH9-based
    . If ICH9, check the interrupt polarity specified in the corresponding RTE entry of IOAPIC. If the polarity is active low, then
      a) Mask this line in the physical IOAPIC, and
      b) Virtualize the IOAPIC and the corresponding RTE entry mask field to the guest OS.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*

7. ICH9 High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level

Problem: During Start-of-Packet (SOP)/End-of-Packet (EOP), the ICH9 may drive D+ and D- lines to a level greater than USB 2.0 spec +/-200mV max.

Implication: May cause High Speed (HS) USB 2.0 devices to be unrecognized by OS or may not be readable/writable if the following two conditions are met:

- The receiver is pseudo differential design
- The receiver is not able to ignore SE1 (single-ended) state

Note: Intel has only observed this issue with a motherboard down HS USB 2.0 device using pseudo differential design. This issue will not affect HS USB 2.0 devices with complementary differential design or Low Speed (LS) and Full Speed (FS) devices

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

8. PET Alerts on SMBus

Problem: When using the ICH9 SMBus for Platform Event Trap (PET) alerts on a system with the Intel® Management Engine (ME) enabled, the SMBus packet headers may be corrupted if all of the following conditions are met:

- SMBus slave is the target of an external PET generating master on SMBus/SMLink
- The ME is in the middle of M0-M1 transitions
- SMBus slave receives back-to-back PET alerts of which some PET alerts are incomplete (i.e. the packet is truncated to less than 6 bytes)

Note: This issue has only been observed under a synthetic test environment.

Implication: ME firmware may stop functioning, which could cause a system hang.

Workaround: None

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

9. SMBus Host Controller May Hang

Problem: During heavy SMBus traffic utilization, the ICH9 SMBus host controller may attempt to start a transaction while the bus is busy.

Note: This issue has only been observed under a synthetic test environment.

Implication: May cause the SMBus host controller to hang.

- After boot:
  - — SMBus host controller transaction may not complete.
  - — External master transaction in progress targeting ICH9 SMBus slave may get NACK or timeout.
  - — There is no impact to any other transaction that was in progress by an external master.
- This issue has not been observed during boot as SMBus utilization tends to be light.

Workaround: BIOS workaroud available.
Contact your Intel field representative for details.

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

10. SATA Gen1 Initialization/LPM Erratum

Problem: During SATA Initialization routines or while resuming from a Link Power Managed (LPM) state, the ICH9 SATA link to Gen1 (1.5 Gb/s) devices may fail to be established.

Implication: One or more of the following symptoms may occur:

- During Boot or Resume from S4/S5: SATA Gen1 devices may not be detected, resulting in "Operating System Not Found" error.
- During Resume from S3: System may hang when attempting to initialize SATA Gen1 devices.
- During S0: If LPM is enabled and ALL SATA Gen1 devices within the system support LPM, slow SATA Gen1 performance may occur.

Workaround: BIOS workaround available.
Contact your Intel field representative for details.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

§ §

Specification Changes

1. t212 Change

The following change applies to Table 8-20 of the Datasheet.

t212	VRMPWRGD active to PWROK active	3	–	ms		8-15 8-17

2. LANRST# Timing

a. The following change applies to Table 2-11 of the Datasheet.

LAN_RST#	I	**LAN Reset:** When asserted, the internal LAN controller is in reset. This signal must be asserted until the LAN power wells (VccLAN3_3 and VccLAN1_05) and VccCL3_3 power well are valid. When deasserted, this signal is an indication that the LAN power wells are stable. **NOTES:** 1. LAN_RST# must not deassert before RSMRST# deasserts 2. LAN_RST# must not deassert after PWROK asserts. 3. LAN_RST# must not deassert until 1 ms after the LAN power wells (VccLAN3_3 and VccLAN1_05) and VccCL3_3 power well are valid. 4. If integrated LAN is not used LAN_RST# can be tied to Vss. 5. LAN_RST# must assert a minimum of 20 ns before LAN power rails become inactive

b. The following change applies to Table 8.21 of the Datasheet.

t305a	LAN Power Rails active to LAN_RST# deassertion	1		ms	18	
t305b	LAN_RST# assertion to LAN power rails inactive	20		ns	25	

25. A power rail is considered to be inactive when the rail is at its nominal voltage minus 5% or less.

3. Removing Support for USB Wake from S5

Support for USB wake from S5 is removed from the Datasheet as indicated below.

a. Update Intel® ICH9 Features page of the Datasheet as follows:

- USB 2.0
  - —NEW: Six UHCI Host Controllers, supporting up to twelve external ports
  - —Two EHCI Host Controllers, supporting up to twelve external ports
  - —Two Configuration Options for EHCI Controllers 6+6 and 8+4
  - —Per-Port-Disable Capability
  - —Includes up to two USB 2.0 High-speed Debug Ports
  - —Supports wake-up from sleeping states S1–S4
  - —Supports legacy Keyboard/Mouse software

Update Table 5-31 as follows:

Table 5-31. Causes of Wake Events

Cause	States Can Wake From	How Enabled
Classic USB	S1–S4	Set USB1_EN, USB 2_EN, USB3_EN, USB4_EN, USB5_EN, and USB6_EN bits in GPE0_EN register

4. Addition of EHCI Parity Error Response

Parity Error Response is supported by the ICH9 Enhanced Host Controller (EHC). The following changes apply to Section 17.1.3 of the Datasheet to reflect the added capability.

8	**SERR# Enable (SERR_EN)** — R/W 0 = Disables EHC's capability to generate an SERR#. 1 = The Enhanced Host Controller (EHC) is capable of generating (internally) SERR# in the following cases: - When it receives a completion status other than "successful" for one of its DMA -initiated memory reads on DMI (and subsequently on its internal interface). - When it detects an address or command parity error and the Parity Error Response bit is set. - When it detects a data parity error (when the data is going into the EHC) and the Parity Error Response bit is set.
6	**Parity Error Response (PER)** — R/W. 0 = The EHC is not checking for correct parity (on its internal interface). 1 = The EHC is checking for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase. **NOTE:** If the EHC detects bad parity on the address or command phases when the bit is set to 1, the host controller does not take the cycle. It halts the host controller (if currently not halted) and sets the Host System Error bit in the USBSTS register. This applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.

5. SATA Port Multipliers Removal

Support for SATA port multipliers in the ICH9 has been removed. References to port multipliers are removed from the Datasheet as indicated below:

- Section Intel® ICH9 Feature: Removing Port Multipliers under External SATA Support.
- Section 5.16.1: Removing Port Multipliers references in the tables.
- Section 14.4.1.1: bit 17 is now Reserved.
- Section 14.4.3.7: bit 17 is now Reserved.

6. CF9 Lock Bit Addition

The following change applies to Section 13.8.1.5 of the Datasheet.

31	**CF9h Lock Down (CF9Lock)**— RW. When set to 1, this bit locks itself and bit 20 (CF9GR) in this register. This bit is reset by a CF9h reset.

Specification Clarifications

1. GLANCLK High Time/Low Time Clarification

The following changes apply to Table 8-8 of the Datasheet:

tglanhi	High Time	6.4		ns		
tglanlo	Low Time	6.4		ns		

2. DC Characteristics Clarifications

a. The following changes apply to Table 8-4 of the Datasheet.

Table 8-4. DC Input Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.5	0.8	V	
V_{IH3}	Input High Voltage	2.0	3.3 V + 0.5	V	Note 12
V_{IL4}	Input Low Voltage	–0.5	0.3(3.3 V)	V	Note 12
V_{IH4}	Input High Voltage	0.5(3.3 V)	3.3 V + 0.5	V	Note 12
V_{IL5}	Input Low Voltage	–0.5	0.8	V	
V_{IH5}	Input High Voltage	2.1	3.3 V + 0.5	V	Note 12
V_{IL6}	Input Low Voltage	-0.5	0.3(3.3 V)	V	Note 12
V_{IH6}	Input High Voltage	0.6(3.3 V)	3.3 V + 0.5	V	Note 12
V_{IL11}	Input Low Voltage	–0.5	0.35(3.3 V)	V	Note 12
V_{IH11}	Input High Voltage	0.65(3.3 V)	3.3 V + 0.5	V	Note 12
V_{IL13}	Input Low Voltage	–0.5	0.8	V	
V_{IH13}	Input High Voltage	2.0	3.3 V + 0.5	V	Note 12

12. 3.3 V refers to VccSus3_3 for signals in the suspend well and to Vcc3_3 for signals in the core well. See Table 3-2 or Table 3-3 for signal and power well association.

b. The following changes apply to Table 8-6 of the Datasheet.

Table 8-6. DC Output Characteristics

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
V_{OL2}	Output Low Voltage	—	0.1(3.3 V)	V	1.5 mA	Note 7
V_{OH2}	Output High Voltage	0.9(3.3 V)	—	V	-1.5 mA	Note 7
V_{OL3}	Output Low Voltage	—	0.4	V	4 mA	
V_{OH3}	Output High Voltage	3.3 V - 0.5	—	V	-2 mA	Note 1 Note 7
V_{OL4}	Output Low Voltage	—	0.4	V	6 mA	
V_{OH4}	Output High Voltage	3.3 V - 0.5	—	V	-2 mA	Note 7
V_{OL5}	Output Low Voltage	—	0.4	V	5 mA	
V_{OH5}	Output High Voltage	3.3 V – 0.5	—	V	-2 mA	Note 7
V_{OL8}	Output Low Voltage	—	0.1(3.3 V)	V	1.5 mA	Note 7
V_{OH8}	Output High Voltage	0.9(3.3 V)	—	V	-0.5 mA	Note 1 Note 7
V_{OL9}	Output Low Voltage	—	0.4	V	6 mA	
V_{OH9}	Output High Voltage	3.3 V - 0.5	—	V	-0.5 mA	Note 7

7. 3.3 V refers to VccSus3_3 for signals in the suspend well and to Vcc3_3 for signals in the core well. See Table 3-2 or Table 3-3 for signal and power well association.

C. The following changes apply to Table 8-7 of the Datasheet.

VccHDA	High Definition Audio Controller Core Voltage	3.135	3.3	3.465	V	1
VccHDA (low voltage 1.5V)	High Definition Audio Controller Low Voltage Mode Core Voltage	1.425	1.5	1.575	V	1

3. USB UHCI Run/Stop Bit Clarification

The following change applies to Section 16.2.1 of the Datasheet.

0	**Run/Stop (RS)** — R/W. When set to 1, the ICH9 proceeds with execution of the schedule. The ICH9 continues execution as long as this bit is set. When this bit is cleared, the ICH9 completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The host controller clears this bit when the following fatal errors occur: consistency check failure, memory access errors. 0 = Stop 1 = Run **NOTE:** This bit should only be cleared if there are no active Transaction Descriptors in the executable schedule or software will reset the host controller prior to setting this bit again.

4. BIOS VSCC and Management Engine VSCC Clarifications

a. The following changes apply to Section 22.1.27 of the Datasheet.

4	**Write Enable on Write Status (LWEWS)** — RW. This register is locked by the Vendor Component Lock (LVCL) bit. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. ***Notes:*** 1. This is not an atomic sequence. If the SPI component's status register is non volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 2. This bit should not be set to '1' if the SPI flash status regiser is non-volatile. This may lead to premature flash wear out. 3. Bit 3 and bit 4 should NOT be both set to '1'.
3	**Lower Write Status Required (LWSR)** — RW. This register is locked by the Vendor Component Lock (LVCL) bit. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. ***Notes:*** 1. This is not an atomic sequence. If the SPI component's status register is non volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 2. This bit should not be set to '1' if the SPI flash status regiser is non-volatile. This may lead to premature flash wear out. 3. Bit 3 and bit 4 should NOT be both set to '1'.
2	**Lower Write Granularity (LWG) —** RW**.** This register is locked by the Vendor Component Lock (LVCL) bit. 0 = 1 Byte 1 = 64 Byte ***Notes:*** 1. If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components. 2. If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a feature page writeable SPI flash.

b. The following changes apply to Section 22.1.28 of the Datasheet.

4	**Write Enable on Write Status (UWEWS)** — RW.This register is locked by the Vendor Component Lock (UVCL) bit. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. ***Notes:*** 1. This is not an atomic sequence. If the SPI component's status register is non volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 2. This bit should not be set to '1' if the SPI flash status regiser is non-volatile. This may lead to premature flash wear out. 3. Bit 3 and bit 4 should NOT be both set to '1'.

3	**Upper Write Status Required (UWSR)** — RW. This register is locked by the Vendor Component Lock (UVCL) bit. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. ***Notes:*** 1. This is not an atomic sequence. If the SPI component's status register is non volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 2. This bit should not be set to '1' if the SPI flash status regiser is non-volatile. This may lead to premature flash wear out. 3. Bit 3 and bit 4 should NOT be both set to '1'.
2	**Upper Write Granularity (UWG) —** RW. This register is locked by the Vendor Component Lock (UVCL) bit. 0 = 1 Byte 1 = 64 Byte 1. If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components. 2. If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a a feature page writeable SPI flash.

c. The following changes apply to Section 22.2.8.2 of the Datasheet.

20	**Lower Write Enable on Write Status (LWEWS)**. 0 = No write to the SPI flash's status register required prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. ***Notes:*** 1. This bit should not be set to '1' if the SPI flash status regiser is non-volatile. This may lead to premature flash wear out. 2. Bit 20 and bit 19 should NOT be both set to '1'
19	**Lower Write Status Required (LWSR)**. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. ***Notes:*** 1. Bit 20 and bit 19 should NOT be both set to '1'. 2. Bit 19 should not be set if the flash part does not support the opcode 50h to unlock the status register.

4	**Upper Write Enable on Write Status (UWEWS)**. 0 = No write to the SPI flash's status register required prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. ***Notes:*** 1. This bit should not be set to '1' if the SPI flash status regiser is non-volatile. This may lead to premature flash wear out. 2. Bit 4 and bit 3 should NOT be both set to '1'.
3	**Upper Write Status Required (UWSR)**. 0 = No requirement to write to the Status Register prior to a write 0 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. ***Notes:*** 1. Bit 4 and bit 3 should NOT be both set to '1'. 2. Bit 3 should not be set if the flash part does not support the opcode 50h to unlock the status register.

d. The following changes apply to Section 22.2.8.4 of the Datasheet.

20	**Lower Write Enable on Write Status (LWEWS)**. 0 = No write to the SPI flash's status register required prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. ***Notes:*** 1. This bit should not be set to '1' if the SPI flash status regiser is non-volatile. This may lead to premature flash wear out. 2. Bit 20 and bit 19 should NOT be both set to '1'.
19	**Lower Write Status Required (LWSR)**. 0 = No requirement to write to the Status Register prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. ***Notes:*** 1. Bit 20 and bit 19 should NOT be both set to '1'. 2. Bit 19 should not be set if the flash part does not support the opcode 50h to unlock the status register.
4	**Upper Write Enable on Write Status (UWEWS)**. 0 = No write to the SPI flash's status register required prior to a write 1 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 06h is the opcode used to unlock the Status register. ***Notes:*** 1. This bit should not be set to '1' if the SPI flash status regiser is non-volatile. This may lead to premature flash wear out. 2. Bit 4 and bit 3 should NOT be both set to '1'.
3	**Upper Write Status Required (UWSR)**. 0 = No requirement to write to the Status Register prior to a write 0 = A write of 00h to the SPI flash's status register is required prior to write and erase to unlock the flash component. 50h is the opcode used to unlock the Status register. ***Notes:*** 1. Bit 4 and bit 3 should NOT be both set to '1'. 2. Bit 3 should not be set if the flash part does not support the opcode 50h to unlock the status register.

5. Causes of SMI#/SCI Clarifications

The following changes apply to Table 5-28 of the Datasheet. (Two items are added to the table and three existing items are modified.)

Table 5-28 Causes of SMI# and SCI

Cause	SCI	SMI	Additional Enables	Where Reported
SW Generated GPE	Yes	Yes	SWGPE_EN=1	SWGPE_STS
SPI Command Completed	No	Yes	FSMIE (See SPI Hardware Sequencing Flash Control Register)	SPI_STS
TCO SMI — Write attempted to BIOS	No	Yes	BIOSWE=1	BIOSWR_STS
TCO SMI — Change of the BIOSWE bit from 0 to 1	No	Yes	BLE=1	BIOSWR_STS
Write attempted to BIOS	No	Yes	BIOSWE = 0	BIOSWR_STS

6. SATA Clock Gating Control Register Clarification

The following change applies to Section 14.1.32 of the Datasheet.

31	Reserved
30	**SATA Clock Request Enabled (SCRE) — RW** 0 = SATA Clock Request Protocol is disabled. SATACLKREQ# pin, when in native function, will always output '0' to keep the SATA clock running. 1 = SATA Clock Request Protocol is enabled. SATACLKREQ# pin, when in native function, will behave as the SATA clock request to the system clock chip.

7. CLIST1 (D25:F0:Offset C8h-C9h) Register Corrections

Bits [15:8] in the CLIST1 register are R/WO bits. The changes are reflected in Table 12-1 and Section 12.1.19 of the Datasheet as follows:

Table 12-1:

C8h–C9h	CLIST1	Capabilities List 1	D001h	RO, R/WO

Section 12.1.19:

Address Offset: C8h–C9h
Default Value: D001h
Attribute: RO, R/WO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)** — R/WO. Value of D0h indicates the location of the next pointer.
7:0	**Capability ID (CID)** — RO. Indicates the linked list item is a PCI Power Management Register.

8. EHCI Initialization Register 1 Clarification

The following change applies to Section 17.1.30 of the Datasheet.

Bit	Description
7:5	Reserved
4	**Pre-fetch Based Pause Disable** — R/W. 0 = Pre-fetch Based Pause is enabled. 1 = Pre-fetch Based Pause is disabled.
3:0	Reserved

9. PCI Express* Root Port Configuration Register Clarification

The following change applies to Section 10.1.40 of the Datasheet.

2	**Port Configuration2 (PC2)** — R/W. This controls how the PCI bridges are organized in various modes of operation for Ports 5 and 6. 1 = Reserved 0 = 2 x1s, Port 5 (x1), Port 6 (x1) This bit is in the resume well and is only reset by RSMRST#. Note: Writing to this bit is for debug/testing only. This bit should be treated as Read Only and modifiable only through the GNT2# / GPIO53 pin strap
1:0	**Port Configuration (PC)** — R/W. This controls how the PCI bridges are organized in various modes of operation for Ports 1-4. For the following mappings, if a port is not shown, it is considered a x1 port with no connection. These bits represent the strap values of HDA_SDOUT (bit 1) and HDA_SYNC (bit 0) when TP[3] is not pulled low at the rising edge of PWROK. 11 = 1 x4, Port 1 (x4) 10 = Reserved 01 = Reserved 00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1), Port 4 (x1) These bits live in the resume well and are only reset by RSMRST#. Note: Writing to these bits is for debug/testing only. These bits should be treated as Read Only and modifiable only through the HDA_SDOUT and HDA_SYNC pin straps

Documentation Changes

1. PWROK Description Correction

The following change applies to Section 5.13.10.3 of the Datasheet.

The PWROK input should go active no sooner than 99 ms after the core supply voltages become valid. PWROK must not glitch, even if RSMRST# is low.

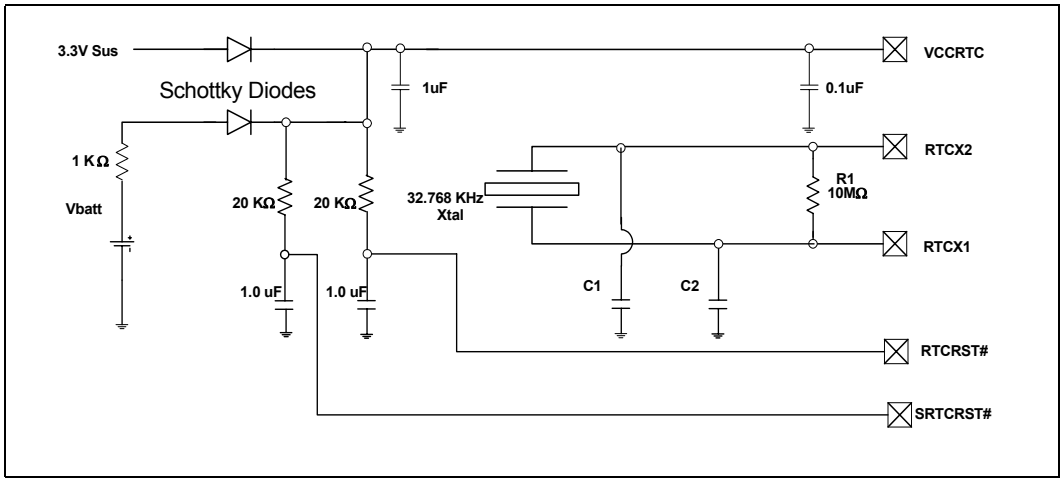
2. SMBus/SMLink Connectivity Clarification

The following change applies to the 4th paragraph in Section 5.20.1 of the Datasheet.

The ICH8 supports the *System Management Bus (SMBus) Specification,* Version 2.0. Slave functionality, including the Host Notify protocol, is available on the SMBus pins. The SMLink and SMBus signals can be tied together externally depending on the TCO mode used. Refer to Section 5.14.2 for more details.

3. External RTC Circuit Correction

The following figure replaces Figure 2-2 of the Datasheet.



4. D31:F6:52h Register Default Value Correction

The following change applies to Section 23.1.22 of the Datasheet.

23.1.22 PC- Power Management Capabilities

Address Offset:	52h–53h	Attribute:	RO
Default Value:	0023h	Size:	16 bits

5. SPI_CS0# Description Correction

The reference to a functional strap is removed from the SPI_CS0# description in Section 2.19 of the Datasheet as indicated below.

SPI_CS0#	O	**SPI Chip Select 0**: Used as the SPI bus request signal.

6. Miscellaneous Register Default Value Corrections

a. The following change applies to Section 13.10.6 of the Datasheet.

13.10.6 GP_SB_CMDSTS [31:0] - GP Serial Blink Command Status [31:0]

Address Offset:	GPIOBASE + 20h	Attribute:	R/W, RO
Default Value:	00080000h	Size:	32 bits
Lockable:	No	Power Well	Core

b. The following change applies to Section 13.10.10 of the Datasheet.

13.10.10 GP_IO_SEL2 - GPIO Input/Output Select 2 [60:32]

Address Offset:	GPIOBASE + 34h	Attribute:	R/W
Default Value:	1B55FFF0h	Size:	32 bits
Lockable:	Yes	Power Well:	Core for 0:7, 16:23 Resume for 8:15, 24:31

c. The following change applies to Table 21-1 and Section 21.1.1 of the Datasheet.

Table 21-1

000-007h	GCAP_ID	General Capabilities and Identification	0429B17F8086A301h	RO

21.1.1 GCAP_ID - General Capabilities and Identification Register

Address Offset:	00h	Attribute:	RO
Default Value:	0429B17F8086A301h	Size:	64 bits

7. Miscellaneous Electrical Correction

In Table 8-6 of the Datasheet, I_{OH2} is changed from -1.5 mA to -0.5 mA.

8. HPET Address Range Correction

The fourth memory address range for HPET given in the introduction of Chapter 21 of the Datasheet is changed from FED0_4000h to FED0_3000h.

9. GNT[3:0]# Pull-Up Enable Correction

The following change applies to Note 12 of Table 3-1 of the Datasheet.

12. The Pull-up on this signal is enabled when the core power is valid.

10. Device 31 Interrupt Pin Register Corrections

The following changes apply to Section 10.1.54 of the Datasheet.

Bit	Description
27:24	**Thermal Throttle Pin (TTIP)** — R/W. Indicates which pin the Thermal Throttle controller drives as its interrupt 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# (Default) 4h = INTD# 5h-Fh = Reserved
15:12	**SM Bus Pin (SMIP)** — R/W. Indicates which pin the SMBus controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# (Default) 4h = INTD# 5h-Fh = Reserved

11. D31:F0 Capability List Pointer Addition

The following register is added as a new section, 13.1.12, in the Datasheet.

13.1.12 CAPP - Capability List Pointer

Offset Address: 34h
Default Value: E0h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Capability Pointer (CP)** — RO. Indicates the offset of the first Capability Item.

§ §